

High Speed, Low Power Monolithic Op Amp

AD847

FEATURES

Superior Performance
- High Unity Gain BW: 50 MHz
- Low Supply Current: 5.3 mA
- High Slew Rate: 300 V/μs
- Excellent Video Specifications
  - 0.04% Differential Gain (NTSC and PAL)
  - 0.19° Differential Phase (NTSC and PAL)
- Drives Any Capacitive Load
- Fast Settling Time to 0.1% (10 V Step): 65 ns

Excellent DC Performance
- High Open-Loop Gain 5.5 V/mV (R_{LOAD} = 1 kΩ)
- Low Input Offset Voltage: 0.5 mV

Specified for ±5 V and ±15 V Operation

Available in a Wide Variety of Options
- Plastic DIP and SOIC Packages
- Cerdip Package
- Die Form
- MIL-STD-883B Processing
- Tape & Reel (EIA-481A Standard)

Dual Version Available: AD827 (8 Lead)

Enhanced Replacement for LM6361

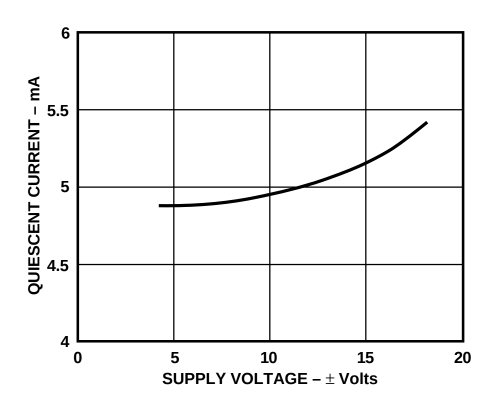
Replacement for HA2544, HA2520/2/5 and EL2020

APPLICATIONS

- Video Instrumentation
- Imaging Equipment
- Copiers, Fax, Scanners, Cameras
- High Speed Cable Driver
- High Speed DAC and Flash ADC Buffers

PRODUCT DESCRIPTION

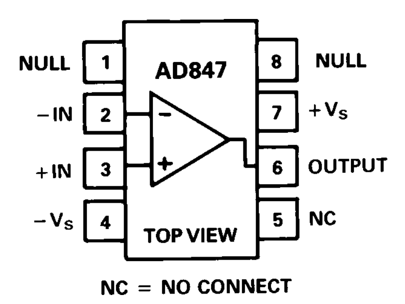
The AD847 represents a breakthrough in high speed amplifiers offering superior ac & dc performance and low power, all at low cost. The excellent dc performance is demonstrated by its ±5 V specifications which include an open-loop gain of 3500 V/V (500 Ω load) and low input offset voltage of 0.5 mV. Common-mode rejection is a minimum of 78 dB. Output voltage swing is ±3 V into loads as low as 150 Ω. Analog Devices also offers over 30 other high speed amplifiers from the low noise AD829 (1.7 nV/√Hz) to the ultimate video amplifier, the AD811, which features 0.01% differential gain and 0.01° differential phase.



Quiescent Current vs. Supply Voltage

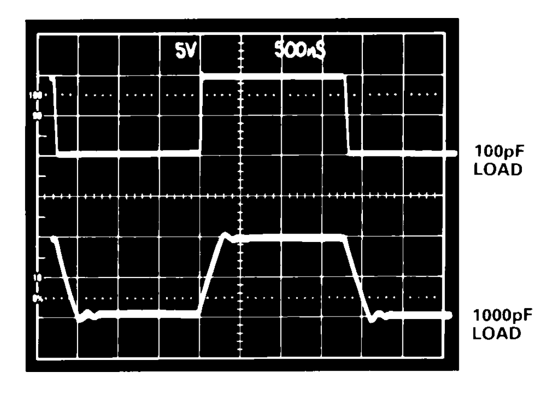
CONNECTION DIAGRAM

Plastic DIP (N), Small Outline (R) and Cerdip (Q) Packages



APPLICATION HIGHLIGHTS

1. As a buffer the AD847 offers a full-power bandwidth of 12.7 MHz (5 V p-p with ±5 V supplies) making it outstanding as an input buffer for flash A/D converters.
2. The low power and small outline package of the AD847 make it very well suited for high density applications such as multiple pole active filters.
3. The AD847 is internally compensated for unity gain operation and remains stable when driving any capacitive load.



AD847 Driving Capacitive Loads

REV. F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD847–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD847J			AD847AR			Units
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**6.6**	µA
	T_{MIN} to T_{MAX}				7.2			10	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		**50**	**300**	nA
	T_{MIN} to T_{MAX}				400			500	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	–2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = –1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	–2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = –1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD}= 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**78**	95		**78**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**78**	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				–3.4			–3.4		V
		±15 V		+14.3			+14.3		V
				–13.4			–13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**6.0**	mA
	T_{MIN} to T_{MAX}				7.3			7.3	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				7.6			7.6	mA

NOTES

[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.

[3]Slew Rate is measured on rising edge.

All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.

Specifications subject to change without notice.

Model	Conditions	V_S	AD847AQ Min	AD847AQ Typ	AD847AQ Max	AD847S Min	AD847S Typ	AD847S Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				**4**			**4**	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**5**		3.3	**5**	µA
	T_{MIN} to T_{MAX}				**7.5**			**7.5**	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		**50**	**300**	nA
	T_{MIN} to T_{MAX}				**400**			**400**	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{MIN} to T_{MAX}		**1**			**1**			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{MIN} to T_{MAX}		**1.5**			**1.5**			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	–2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = –1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	–2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = –1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD}= 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**80**	95		**80**	95		dB
	V_{CM} = ±12 V	±15 V	**80**	95		**80**	95		dB
	T_{MIN} to T_{MAX}		**75**			**75**			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		**72**			**72**			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				–3.4			–3.4		V
		±15 V		+14.3			+14.3		V
				–13.4			–13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**5.7**		4.8	**5.7**	mA
	T_{MIN} to T_{MAX}				**7.0**			**7.8**	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				**7.6**			**8.4**	mA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . 1.2 Watts
  Small Outline (R) . . . . 0.8 Watts
  Cerdip (Q) . . . . 1.1 Watts
Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . ±6 V
Storage Temperature Range (Q) . . . . –65°C to +150°C
  (N, R) . . . . –65°C to +125°C
Junction Temperature . . . . 175°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

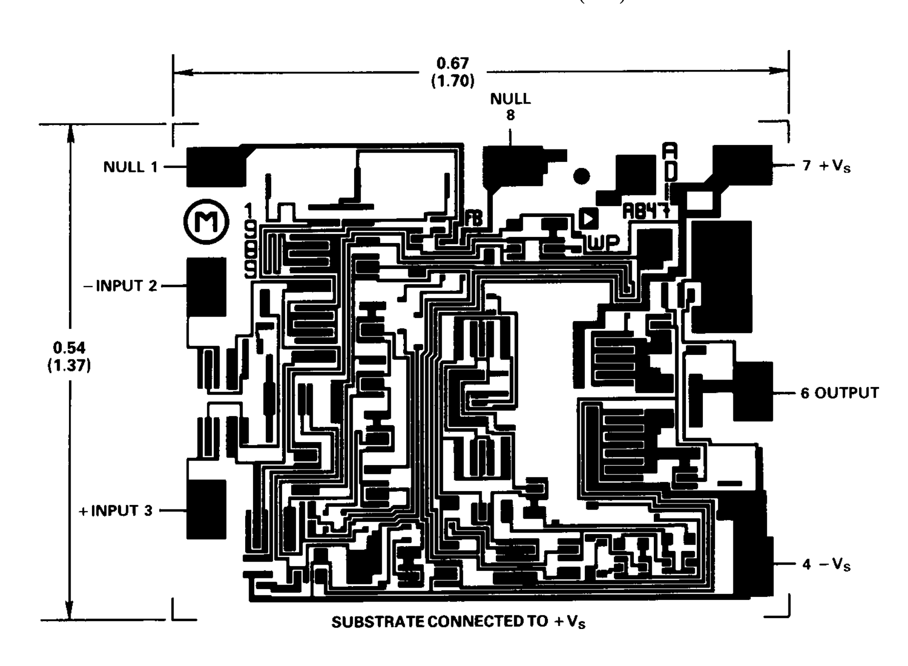
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt; θ_{JC} = 33°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD847 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Models*	Temperature Range – °C	Package Description	Package Option
AD847JN	0 to +70	Plastic	N-8
AD847JR	0 to +70	SOIC	R-8
AD847AQ	–40 to +85	Cerdip	Q-8
AD847AR	–40 to +85	SOIC	R-8
AD847SQ	–55 to +125	Cerdip	Q-8
AD847SQ/883B	–55 to +125	Cerdip	Q-8
5962-8964701PA	–55 to +125	Cerdip	Q-8

*AD847 also available in J and S grade chips, and AD847JR and AD847AR are available in tape and reel.

Typical Characteristics (@ +25°C and $V_S = \pm 15$ V, unless otherwise noted)

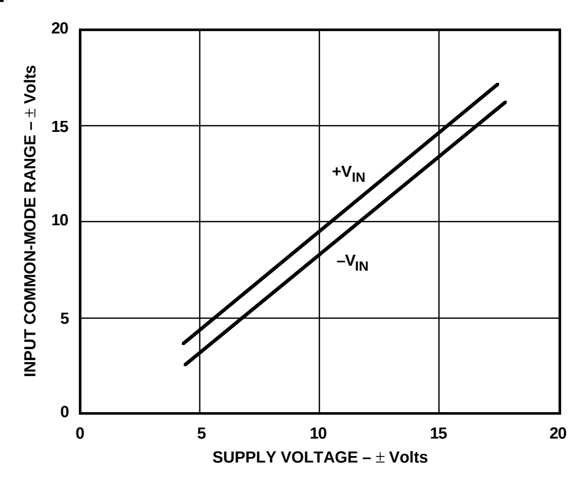


Figure 1. Input Common-Mode Range vs. Supply Voltage

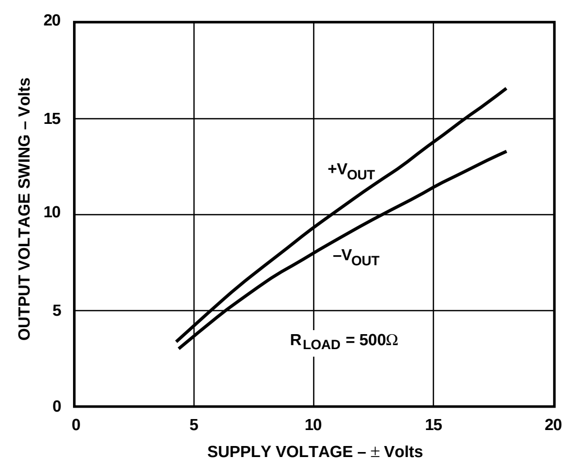


Figure 2. Output Voltage Swing vs. Supply Voltage

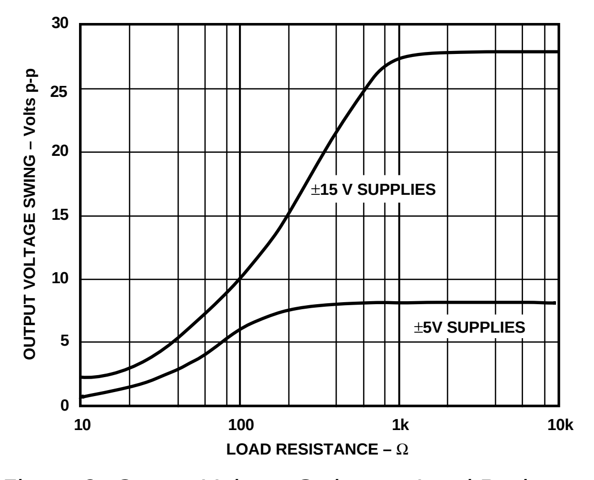


Figure 3. Output Voltage Swing vs. Load Resistance

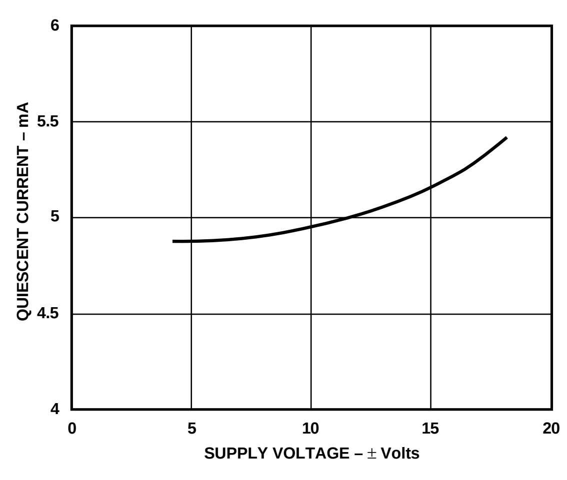


Figure 4. Quiescent Current vs. Supply Voltage

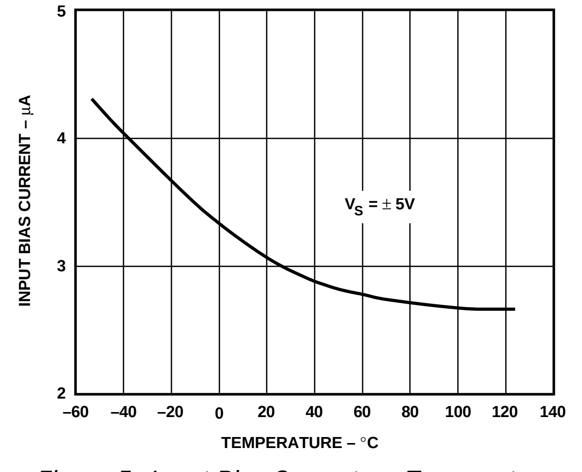


Figure 5. Input Bias Current vs. Temperature

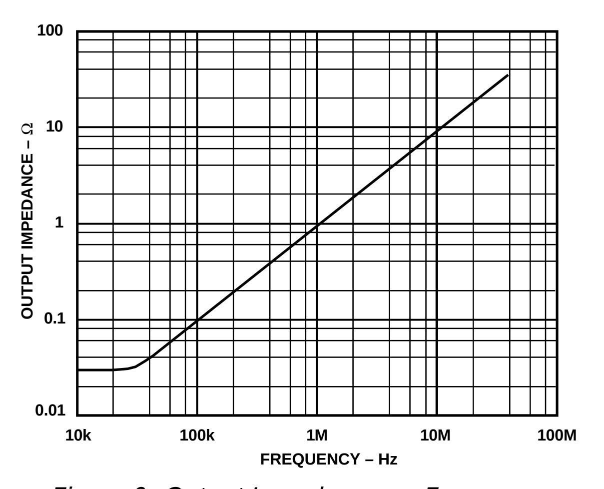


Figure 6. Output Impedance vs. Frequency

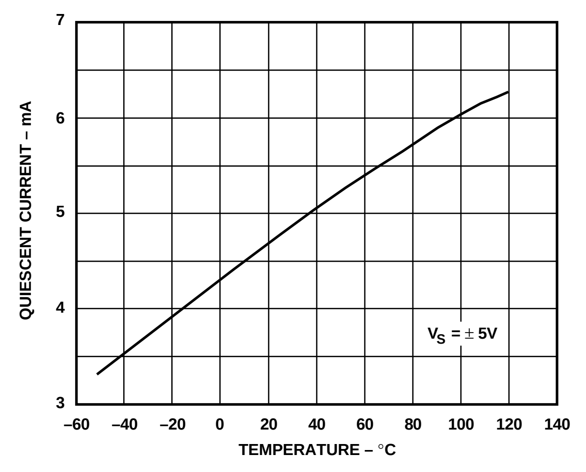


Figure 7. Quiescent Current vs. Temperature

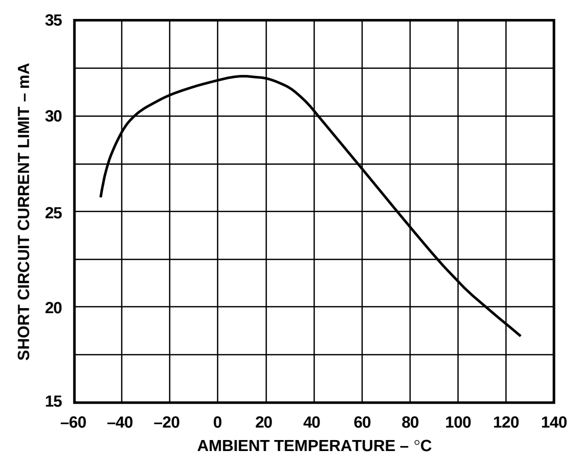


Figure 8. Short-Circuit Current Limit vs. Temperature

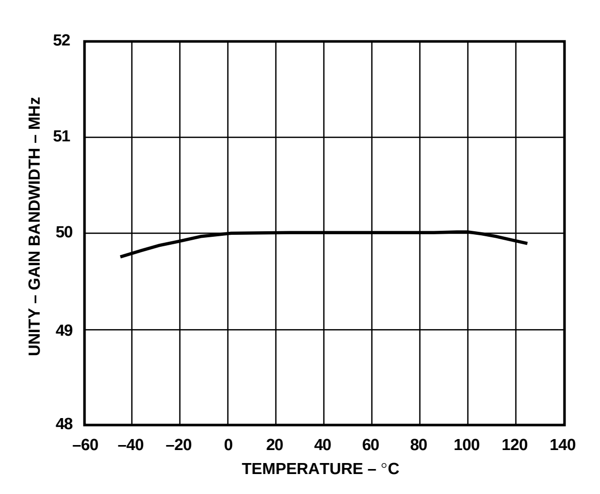


Figure 9. Gain Bandwidth Product vs. Temperature

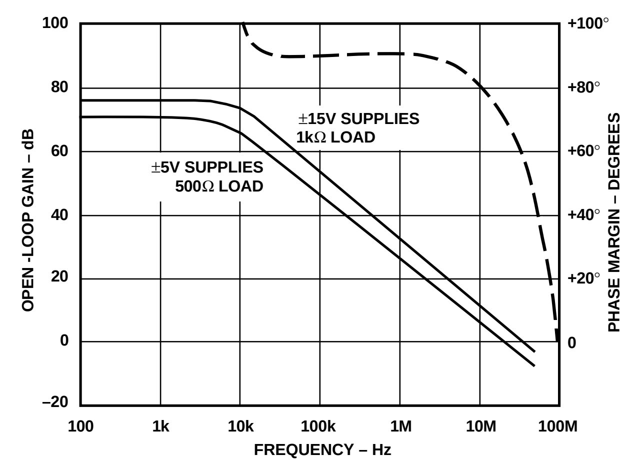


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

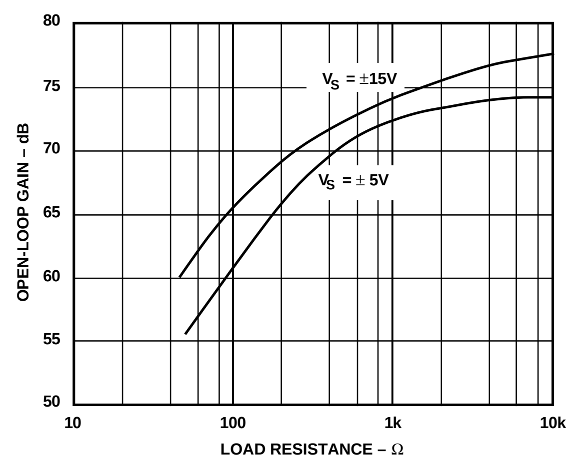


Figure 11. Open-Loop Gain vs. Load Resistance

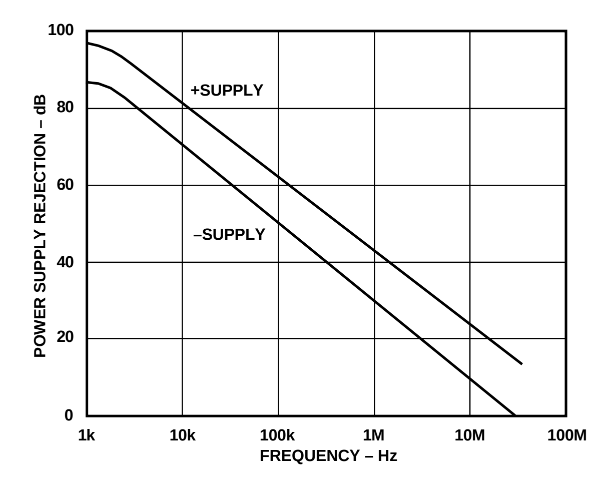


Figure 12. Power Supply Rejection vs. Frequency

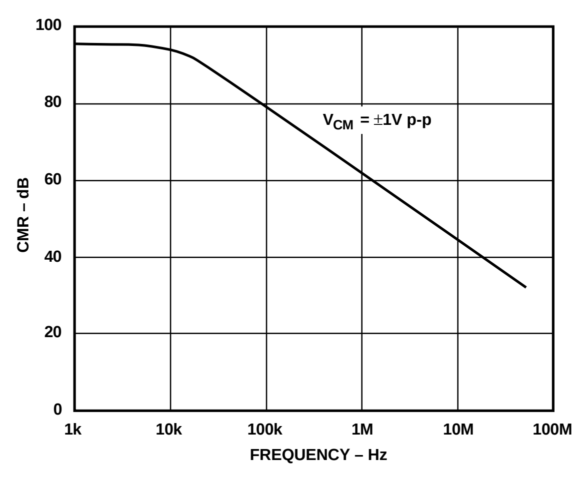


Figure 13. Common-Mode Rejection vs. Frequency

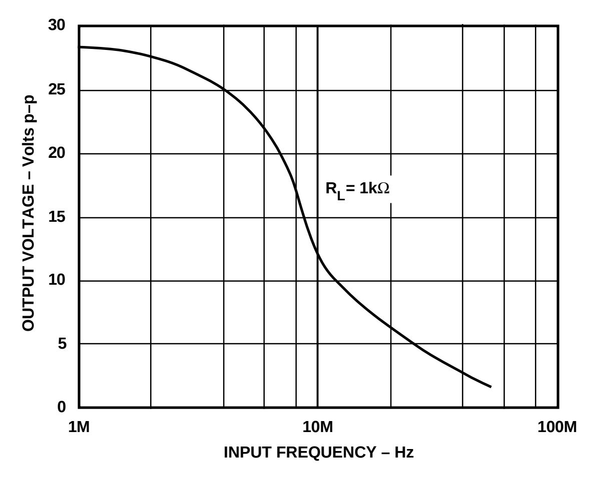


Figure 14. Large Signal Frequency Response

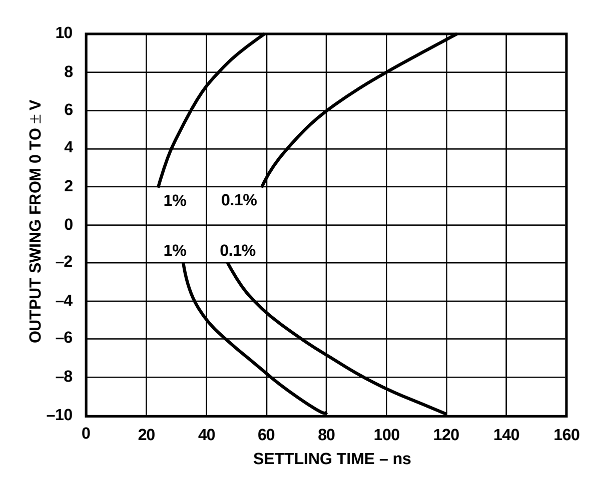


Figure 15. Output Swing and Error vs. Settling Time

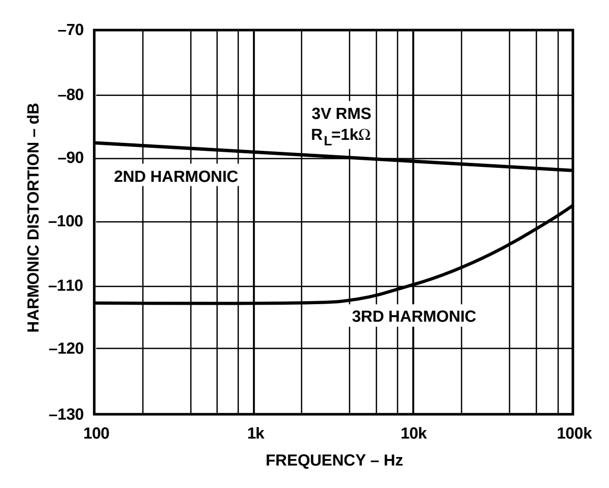


Figure 16. Harmonic Distortion vs. Frequency

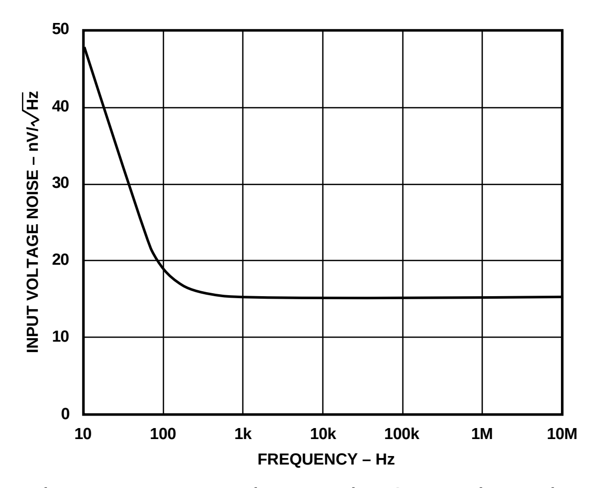


Figure 17. Input Voltage Noise Spectral Density

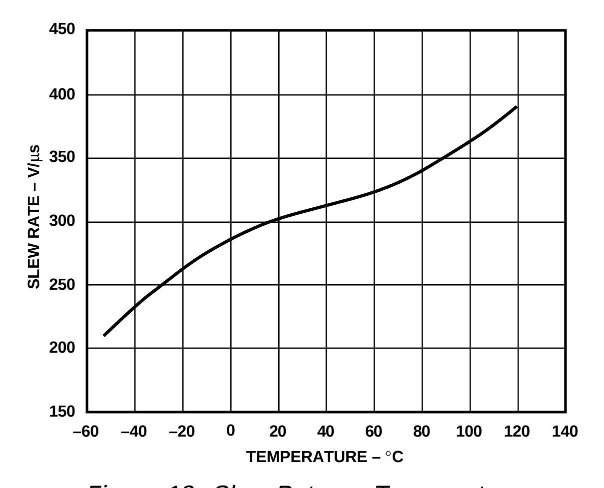


Figure 18. Slew Rate vs. Temperature

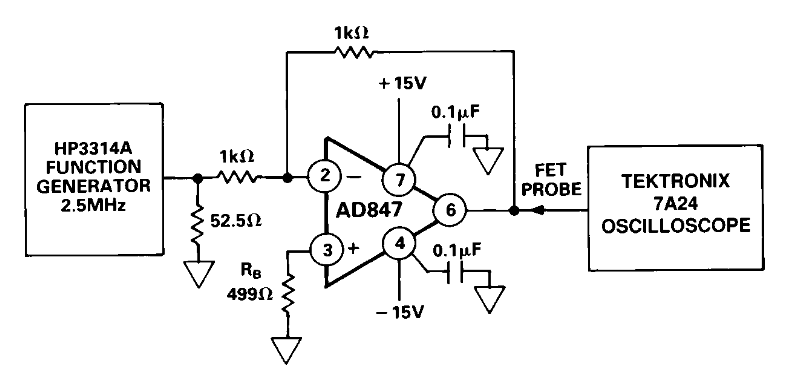


Figure 19. Inverting Amplifier Configuration

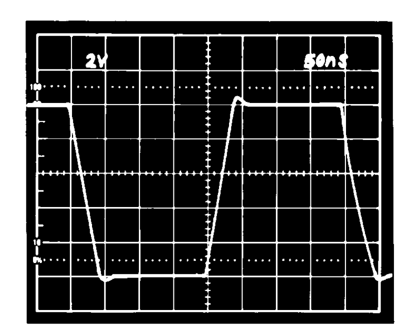


Figure 19a. Inverter Large Signal Pulse Response

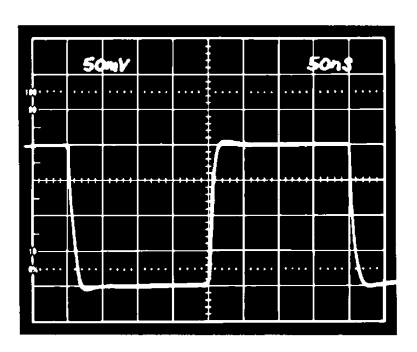


Figure 19b. Inverter Small Signal Pulse Response

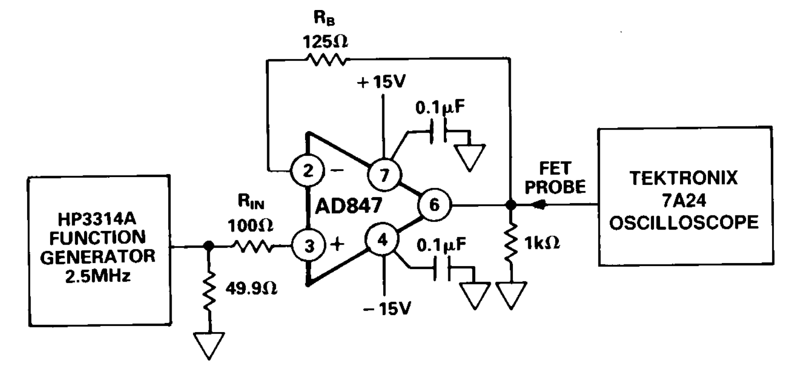


Figure 20. Noninverting Amplifier Configuration

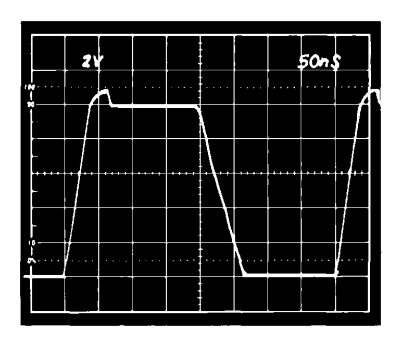


Figure 20a. Noninverting Large Signal Pulse Response

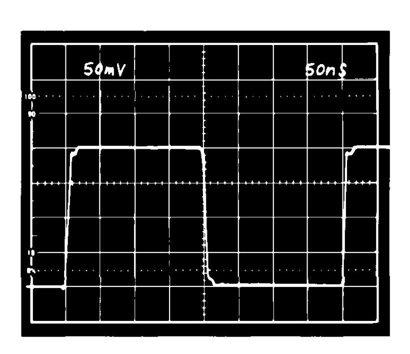


Figure 20b. Noninverting Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD847 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

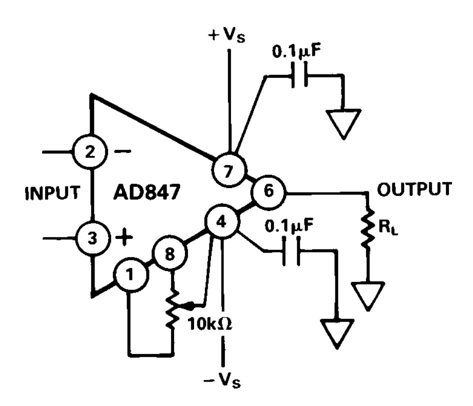


Figure 21. Offset Nulling

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is required in circuits where the input to the AD847 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error will be reduced by more than an order of magnitude.

THEORY OF OPERATION

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_Ts in the 600 MHz to 800 MHz region. The AD847 circuit (Figure 22) includes an npn input stage followed by fast pnps in the folded cascode intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.

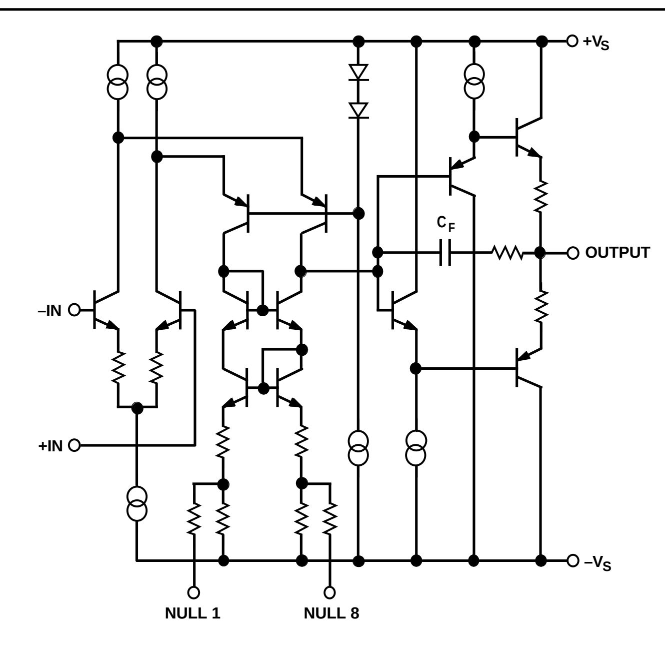


Figure 22. AD847 Simplified Schematic

GROUNDING AND BYPASSING

In designing practical circuits with the AD847, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitance at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 µF are recommended.

VIDEO LINE DRIVER

The AD847 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD847 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD847 maintains a typical slew rate of 200 V/µs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

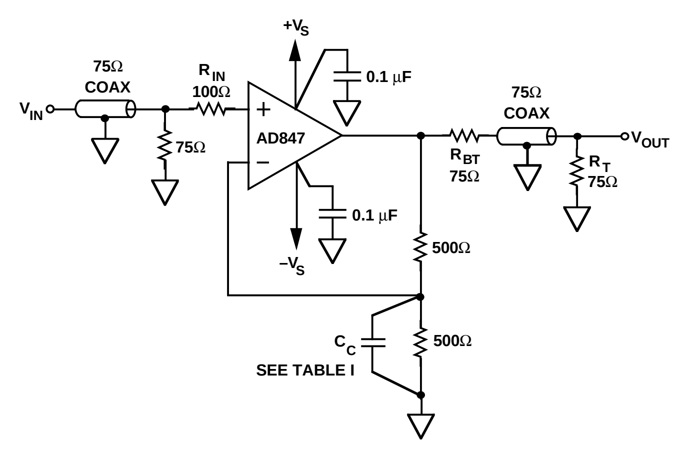


Figure 23. Video Line Driver

Table I. Video Line Driver Performance Chart

V_{IN}*	V_{SUPPLY}	C_C	–3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

*–3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 volt step input.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD847 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

Figure 24 shows the AD847 driving 100 pF and 1000 pF loads.

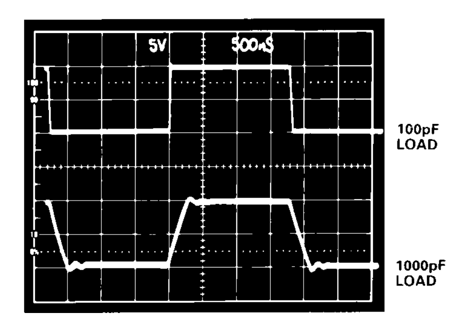


Figure 24. AD847 Driving Capacitive Loads

FLASH ADC INPUT BUFFER

The 35 MHz unity gain bandwidth of the AD847 makes it an excellent choice for buffering the input of high speed flash A/D converters, such as the AD9048.

Figure 25 shows the AD847 as a unity inverter for the input to the AD9048.

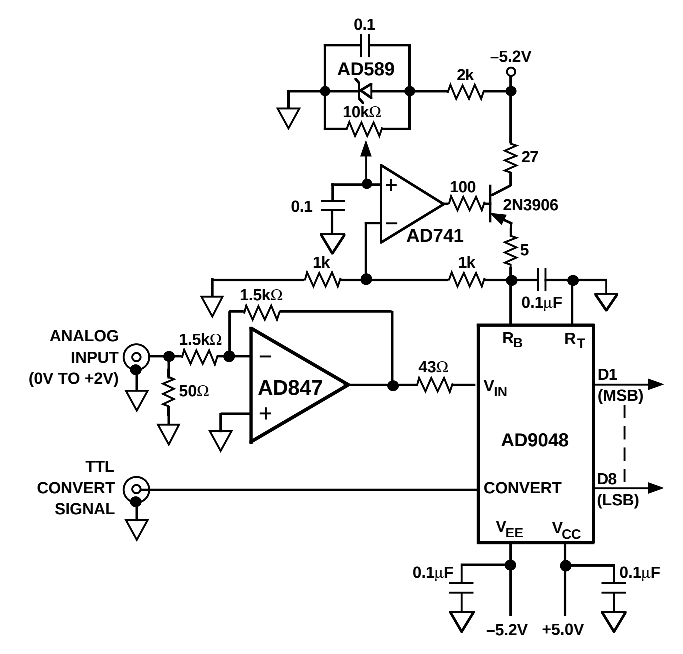
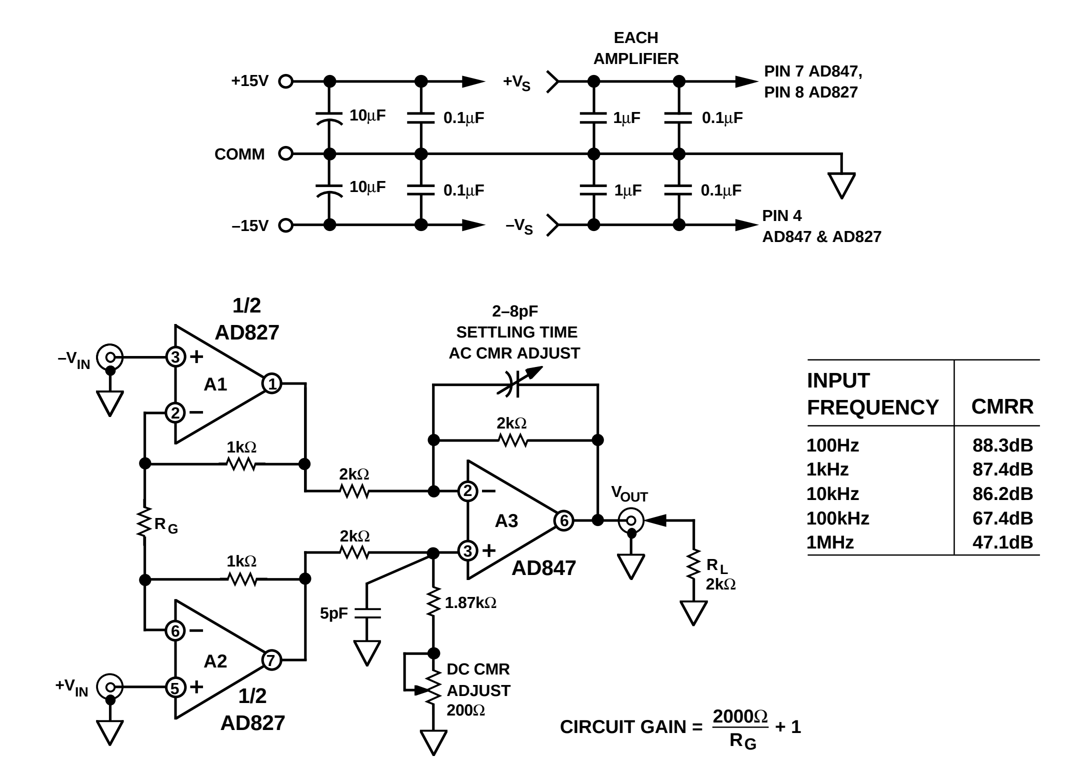


Figure 25. Flash ADC Input Buffer

A High Speed, Three Op-Amp In-Amp

The circuit of Figure 26 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op-amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.



INPUT FREQUENCY	CMRR
100Hz	88.3dB
1kHz	87.4dB
10kHz	86.2dB
100kHz	67.4dB
1MHz	47.1dB

BANDWIDTH, SETTLING TIME AND TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	C_{ADJ} (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
1	OPEN	2–8	16.1MHz	200ns	82dB
2	2kΩ	2–8	14.7MHz	200ns	82dB
10	226Ω	2–8	4.5MHz	370ns	81dB
100	20Ω	2–8	660kHz	2.5µs	71dB

Figure 26. A High Speed In-Amp Circuit for Data Acquisition

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD847 makes it a very good output buffer for high speed current-output D/A converters like the AD668. As shown in Figure 27, the op amp establishes a summing node at ground for the DAC output. The output voltage is determined by the amplifier's feedback resistor (10.24 V for a 1 kΩ resistor). Note that since the DAC generates a positive current to ground, the voltage at the amplifier output will be negative. A 100 Ω series resistor between the noninverting amplifier input and ground minimizes the offset effects of op amp input bias currents.

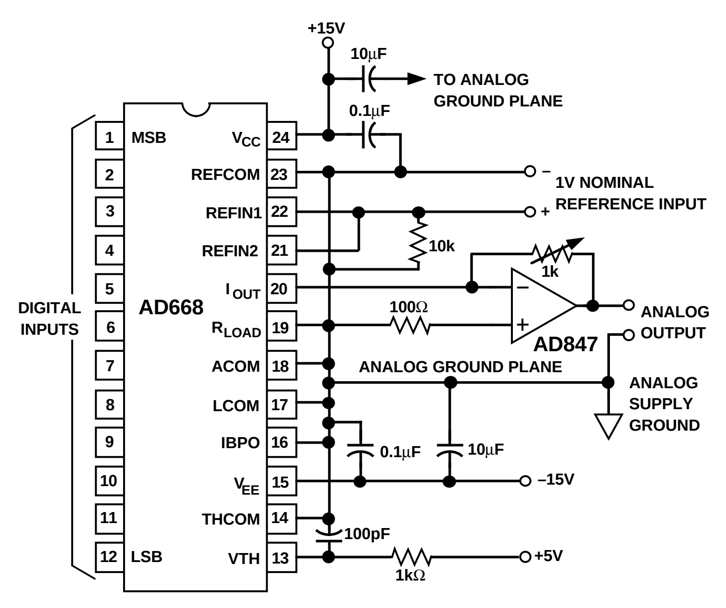


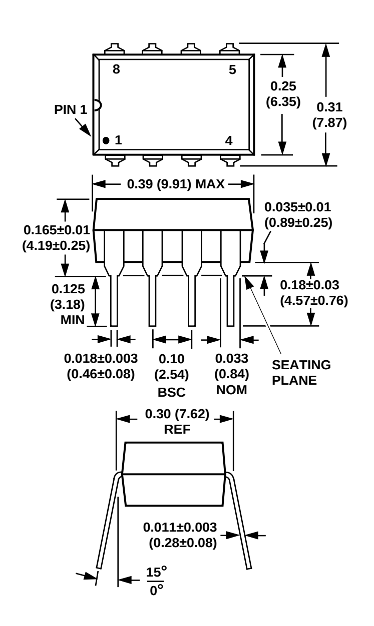
Figure 27. High Speed DAC Buffer

C1191f–10–9/92

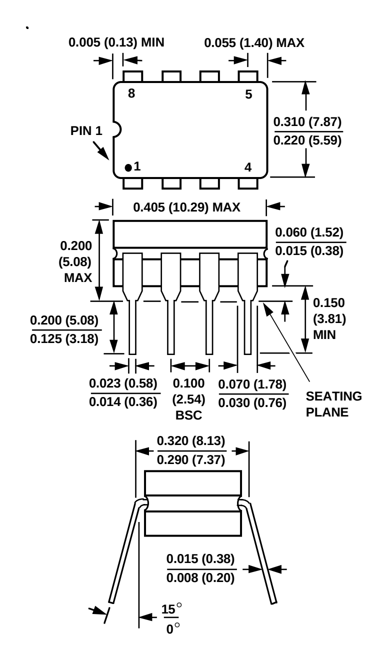
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

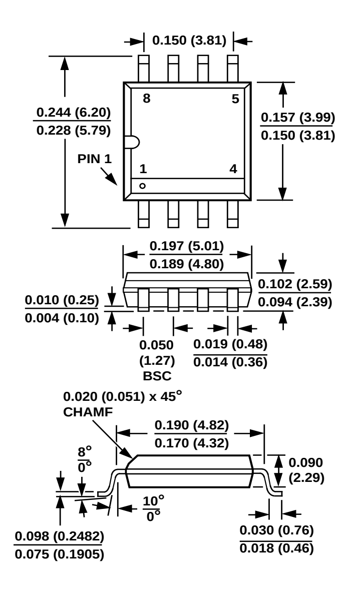
Mini-DIP (N-8) Package



Cerdip (Q-8) Package



Small Outline (R-8) Package



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